UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,580	04/13/2001	Joel Zvi Apisdorf	ACRN-003/00US	5628

26384 7590 12/23/2004		EXAMINER
NAVAL RESEARCH LABORATORY		TSAI, HENRY
ASSOCIATE COUNSEL (PATENTS)		
CODE 1008.2		ART UNIT PAPER NUMBER
4555 OVERLOOK AVENUE, S.W.		2183
WASHINGTON, DC 20375-5320		

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/833,580	APISDORF ET AL.
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _21 October 2004_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-10 and 12-30_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _15-22 and 24-30_ is/are allowed.

6)☒ Claim(s) _1-10, 12-14 and 23_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent,
published under section 122(b), by another filed in the United States
before the invention by the applicant for patent or (2) a patent granted on
an application for patent by another filed in the United States before the
invention by the applicant for patent, except that an international
application filed under the treaty defined in section 351(a) shall have the
effects for purposes of this subsection of an application filed in the
United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English
language.

2.   Claims 1-10, 14, and 23 are rejected under 35 U.S.C. 102(e)

as being anticipated by Akkary et al. (U.S. Patent No.

6,182,210) hereafter referred to as Akkary et al.

Referring to claim 1, Akkary et al. discloses as claimed an

apparatus for instruction-level parallelism in a processing

element, comprising: an instruction control unit (control

circuitry 224A, see Fig. 10); a first instruction buffer

(instruction queue array 202A, see Fig. 10) coupled to said

instruction control unit (control circuitry 224A, see Fig. 10);

a second instruction buffer (instruction queue array 202A, see

Fig. 10, see also col. 9, lines 48-52, regarding instructions

are written into different trace buffer (comprising different

instruction queue array 202A therein) or into instruction queue

array 202A at a different time) coupled to said instruction

control unit; a dependency counter (data and dependency array

206A including "Relay Count" and "Value" or "Pride" see Fig. 13,

and see also col. 10, lines 58-67, and col. 11, lines 1-34)

coupled to said instruction control unit; an execution switch

(SCHED/ISSUE 156, see Fig. 2) coupled to (best reasonably and

broadly interpreted, see Fig. 2) said instruction control unit

(control circuitry 224A, see Fig. 10), said first instruction

buffer (instruction queue array 202A, see Fig. 10), and said

second instruction buffer (instruction queue array 202A, see

Fig. 10); and an execution unit (EXEC UNITS 158, see Fig. 2)

coupled to said execution switch (SCHED/ISSUE 156, see Fig. 2).

Referring to claim 7, Akkary et al. discloses as claimed an

apparatus for processing; instructions in multiple threads an

execution unit (EXEC UNITS 158, see Fig. 2), comprising: an

instruction buffer (instruction queue array 202A, see Fig. 10)

holding a first instruction and a second instruction (see col.

9, lines 48-52, regarding instructions that are part of another

thread are written into instruction queue array 202A at a

different time), the first instruction being associated with a

first thread, and the second instruction being associated with a

second thread; a dependency counter (data and dependency array

206A see Fig. 10, and see also col. 10, lines 58-67, and col.

11, lines 1-34); an instruction control unit (control circuitry

224A, see Fig. 10) coupled to (see Fig. 10) said instruction

buffer and said dependency counter, said instruction control

unit (control circuitry 224A, see Fig. 10) detecting instruction

dependency bits ("DEPENDENCY FIELD", see Fig. 13) and

incrementing and decrementing said dependency counter ("REPLAY

COUNT", see Fig. 13); and an execution switch (SCHED/ISSUE 156,

see Fig. 2) coupled to (through bus 120A or 126A, see Fig. 10)

said instruction control unit and said instruction buffer, said

execution switch sending instructions to the execution unit

(EXEC UNITS 158, see Fig. 2).

Referring to claim 12, Akkary et al. discloses as claimed

an apparatus for instruction-level parallelism, comprising: an

instruction buffer (instruction queue array 202A, see Fig. 10)

holding a first instruction and a second instruction (see col.

9, lines 48-52, regarding instructions that are part of another

thread are written into instruction queue array 202A at a

different time), the first instruction being associated with a

first thread, and the second instruction being associated with a

second thread; and an instruction control unit (control

circuitry 224A, see Fig. 10) coupled to said instruction buffer,

said instruction control unit (control circuitry 224A, see Fig.

10) detecting instruction dependency bits (the bits in

"DEPENDENCY FIELD", see Fig. 13) that indicate dependency

between an instruction and one or more threads other than the

thread with which the instruction is associated (note

"DEPENDENCY FIELD" in Fig. 13 indicating the dependency between

different instructions based on R1-R4 bits as shown in the

figure), and sending instructions to the execution unit (EXEC

UNITS 158, see Fig. 2) to be executed.

Referring to claim 23, Akkary et al. discloses as claimed a

method for processing instructions in multiple threads

comprising: loading a first instruction associated with a first

thread; detecting (by using control circuitry 224A, see Fig. 10)

dependency between the first instruction and a second

instruction associated with a second thread based on dependency

bits (the bits R1-R4 included in "DEPENDENCY FIELD" see Fig. 13)

in an instruction buffer (see col. 9, lines 48-52, regarding

instructions that are part of another thread are written into

instruction queue array 202A at a different time) and the value

(such as "Relay Count", "Value" or "Pride" see Fig. 13) of a

dependency counter (data and dependency array 206A see Fig. 10).

As to claim 2, Akkary et al. also discloses: the dependency

counter (data and dependency array 206A see Fig. 10) includes a

first counter ("REPLAY COUNT" see Fig. 13) associated with the

first instruction buffer and a second counter associated with

the second instruction buffer. Note as shown in Fig. 13,

different "REPLAY COUNT" and "DEPENDENCY FIELD" are related to

different instructions which may be saved in the first and

second instruction buffers (instruction queue array 202A, see

Fig. 10, see also col. 9, lines 48-52, regarding instructions

are written into different trace buffer (comprising different

instruction queue array 202A therein) or into instruction queue

array 202A at a different time).

As to claim 3, Akkary et al. also discloses: said

instruction control unit identifies instruction dependency bits

("DEPENDENCY FIELD" see Fig. 13) in said first instruction

buffer, the instruction dependency bits being associated with

instructions (see Fig. 13, different "DEPENDENCY FIELD" are

related to different instructions which may be saved in the

first and second instruction buffers).

As to claim 4, Akkary et al. also discloses: said

instruction control unit generating control signals based on the

("DEPENDENCY FIELD" see Fig. 13) and values ("REPLAY COUNT" or

"VALUE OR PRID" see Fig. 13) included in said dependency counter

(data and dependency array 206A see Fig. 10, and see also col.

10, lines 58-67, and col. 11, lines 1-34).

As to claims 5 and 6, Akkary et al. also discloses: said

execution switch (SCHED/ISSUE 156, see Fig. 2) providing

instructions from said first instruction buffer to said

execution unit dependency bits (EXEC UNITS 158, see Fig. 2)

based on control signals (through bus 120A or 126A, see Fig. 10)

from said instruction control unit (control circuitry 224A, see

Fig. 10).

As to claim 8, Akkary et al. also discloses: said

dependency counter (data and dependency array 206A see Fig. 10)

includes a first counter ("REPLAY COUNT" see Fig. 13) associated

with the first thread and a second counter ("REPLAY COUNT" see

Fig. 13) associated with the second thread (see col. 9, lines

48-52, regarding instructions that are part of another thread

are written into instruction queue array 202A at a different

time).

As to claim 9, Akkary et al. also discloses: said

instruction buffer includes the instruction dependency bits

("DEPENDENCY FIELD" see Fig. 13), the instruction dependency

bits being associated with instructions (see Fig. 13, different

"DEPENDENCY FIELD" are related to different instructions).

As to claim 10, Akkary et al. also discloses: said instruction control detects dependency between the first instruction and the second thread based on dependency bits ("DEPENDENCY FIELD" see Fig. 13) in said instruction buffer and a value (such as "REPLAY COUNT" or "VALUE OR PRID" see Fig. 13) of said dependency counter (data and dependency array 206A see Fig. 10).

As to claim 13, Akkary et al. also discloses: said instruction control unit identifies instruction dependency bits in said instruction buffer, the instruction dependency bits being associated with the first instruction and the second instruction (note "DEPENDENCY FIELD" in Fig. 13 indicating the dependency between different instructions based on R1-R4 bits as shown in the figure).

As to claim 14, Akkary et. al. also discloses: said instruction control detects dependency between the first instruction and the second instruction based on dependency bits said instruction buffer (note "DEPENDENCY FIELD" in Fig. 13 indicating the dependency between different instructions based on R1-R4 bits as shown in the figure).

Allowable Subject Matter

3.   Claims 15-22, and 24-30 are allowed.

4.   As set forth in the previous Office Action, the following
is a statement of reasons for the indication of allowable
subject matter: Akkary et al., the closest reference, and the
other prior art do not teach or fairly suggest: decrementing the
counter if said examining indicates that the second instruction
has already been executed (in claim 15);

   incrementing a counter associated with the second thread if
said determining indicates that execution of a second
instruction depends on the execution of the first instruction
(in claims 17, and 19); and

   the instruction control unit configured to disallow
execution of the first instruction if a dependency counter value
is less than a threshold value (in claim 24). Further the
combination of the above limitations with all of the other
limitations in the respective independent claims is not obvious.

Response to Amendment

5.   Applicant's arguments filed 10/21/04 have been fully

considered but they are not deemed to be persuasive.

Regarding the 35 U.S.C. §112, second paragraph problems,

Applicant's response has overcome these objections and

rejections.

As to claim 1, Applicants argue that the dependency counter

is incremented upon the execution of a first instruction in a

first thread on which a second instruction in a second thread

depends (paragraph 0008). Execution of the second instruction

will depend on whether the counter has reached a threshold value

(0023) (page 10, lines 8-11). Examiner realizes the dependency

counter described in the specification. However, the dependency

counter is best reasonably and broadly interpreted as a counter

related to dependency. Note the limitations in the

specification should not be read into the claims.

Regarding the DAD (Data And Dependency) array of Akkary,

Applicants argue that it contains a replay count field for each

instruction in a thread. The replay count of an instruction is

incremented every time that same instruction is replayed in the

pipeline (col. 11, lines 9-12). This has no relation to the

execution of a different instruction from a different thread as

in the present claim 1. The DAD array's single-bit flags show

relationships between registers and instructions in the thread

(col. 11, lines 18-27), not between instructions in different

threads (page 10, lines 15-21). Examiner disagrees with

Applicants. As set forth in the art rejections above, Akkary et

al. discloses as claimed an apparatus comprising: an instruction

buffer (instruction queue array 202A, see Fig. 10) holding a

first instruction and a second instruction (see col.9, lines 48-

52, regarding instructions that are part of another thread are

written into instruction queue array 202A at a different time).

Therefore, The DAD array's single-bit flags can be interpreted

to show the relationships between instructions in different

threads.

Applicants argue that a given instruction queue array of

Akkary never holds instructions from two different threads at

the same time, as recited in the current claim 12 (page 11,

lines 16-17). Examiner disagrees with Applicants. Note holding

instructions from two different threads at the same time is not

described in the claim language. Claim 12 is best reasonably

and broadly interpreted.

Applicants also argue that the dependency field indicates

relationships between registers and instructions, not between

instructions of different threads (page 11, lines 23-24).

Examiner disagrees with Applicants. As set forth above,
Akkary et al. discloses as claimed an apparatus comprising: an
instruction buffer (instruction queue array 202A, see Fig. 10)
holding a first instruction and a second instruction (see col.9,
lines 48-52, regarding instructions that are part of another
thread are written into instruction queue array 202A at a
different time). Therefore, The DAD array's single-bit flags can
be interpreted to show the relationships between instructions in
different threads.

As to claim 23, Applicants also argue that the Examiner
pointed to the dependency field of Akkary as anticipating the
dependency bits. As explained above the dependency field is
different from the dependency bits (page 12, lines 1-2).
Examiner disagrees with Applicants. As set forth in the art
rejections, as shown in figure 13, "DEPENDENCY FIELD" comprises
bits R1-R4. The "DEPENDENCY FIELD" is reasonably interpreted as
the dependency bits as claimed.

As to claim 23, Applicants further argue that the value or
PRID is the result of a calculation by a single instruction or a
reference to a register containing such a value (col. 11, lines
1-3). This is not related to dependencies between instructions
(page 12, lines 5-7). Examiner disagrees with Applicants. As
set forth in the art rejections, the value such as "Relay

Count", "Value" or "Pride" of the data and dependency array

206A, see Fig. 13, is broadly interpreted as the value of a

dependency counter as claimed. Note basically, all values

inside the data dependency array 206A are related to

dependencies between instructions (see different Instruction IDs

as shown in Fig. 13).

Conclusion

6.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the

extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action

is set to expire THREE MONTHS from the mailing date of this

action. In the event a first reply is filed within TWO MONTHS

of the mailing date of this final action and the advisory action

is not mailed until after the end of the THREE-MONTH shortened

statutory period, then the shortened statutory period will

expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated

from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than

SIX MONTHS from the mailing date of this final action.

Contact Information

7.   Any inquiry concerning this communication or earlier
communications from the examiner should be directed to Dr. Henry
Tsai whose telephone number is (571) 272-4176. The examiner can
normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.
If attempts to reach the examiner by telephone are unsuccessful,
the examiner supervisor, Eddie Chan, can be reached on (571)
272-4162. Any inquiry of a general nature or relating to the
status of this application or proceeding should be directed to
the TC central telephone number, 571-272-2100.

8.   In order to reduce pendency and avoid potential delays,
Group 2100 is encouraging FAXing of responses to Office actions
directly into **the Group at fax number: 703-872-9306.** This
practice may be used for filing papers not requiring a fee. It
may also be used for filing papers which require a fee by
applicants who authorize charges to a PTO deposit account.
Please identify the examiner and art unit at the top of your
cover sheet. Papers submitted via FAX into Group 2100 will be
promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
December 12, 2004